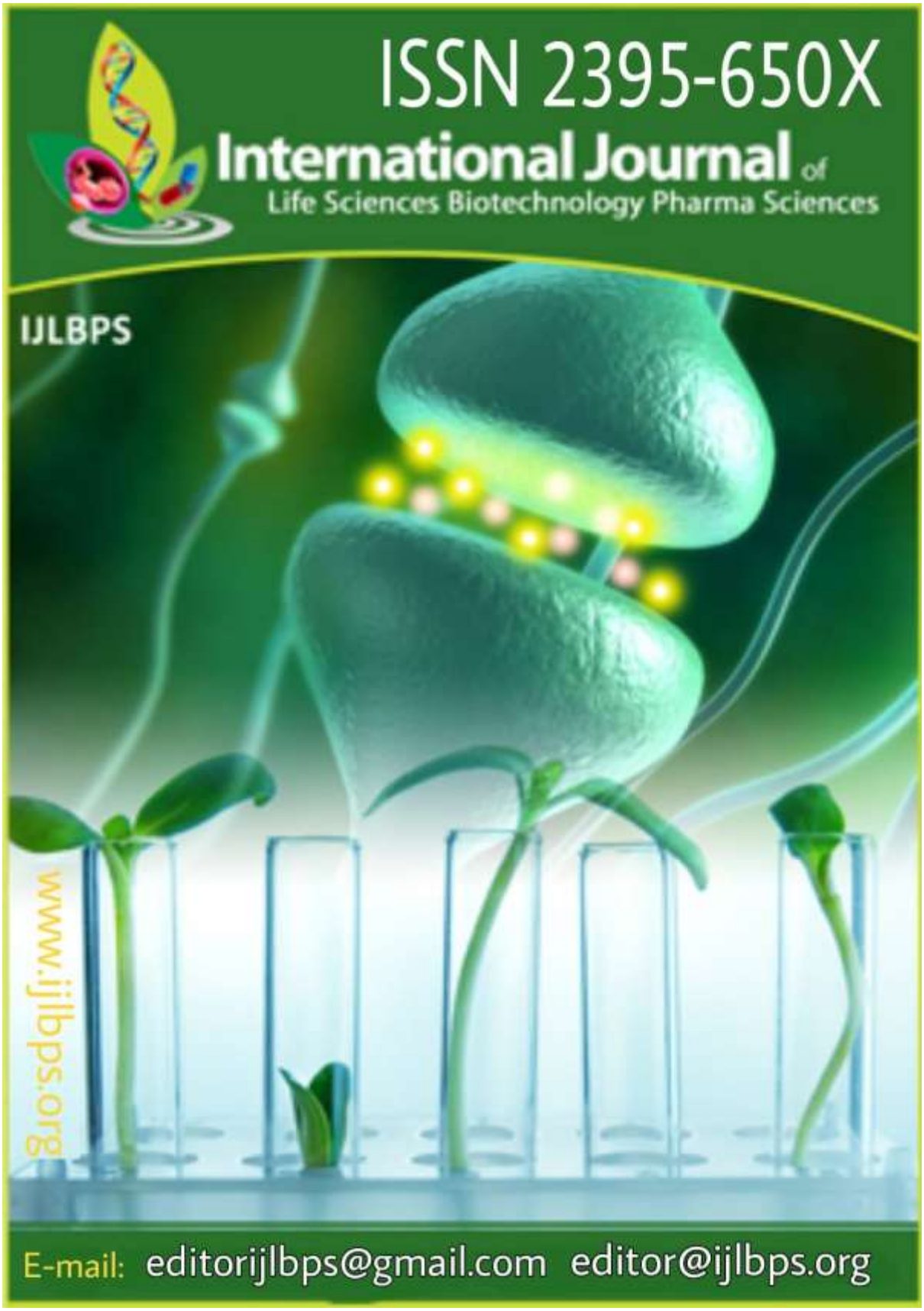
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VERILOG BASED AMBA AXI PROTO COL

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Abstract-Thispapermainlyfocusesonverifying the important features of advancedextensibleinterface(AXI).Verifyingthememory transactions of AX I includes theverificationofallthefivechannelswriteaddress,writedata,writeresponse,readaddressandreaddata.InthisworkaVerificationIntellectualPropertycores(VIP)based methodology is used to carry out theverification Process. In the VIP design theentiretestenvironmentismodeledusingsystemverilogandtheread,writetransactionsfromthesameanddifferentmemory locations has been verified with thequantitativevaluesofBusyCount,ValidCount and its Bus Utilization. Verifying theSystem connectivity during write and readcyclesisalsooneofthefundamentalfeaturesverifiedin this paper.

KEYWORDS:WRITEANDREADTRANSACTIONS,AXIPROTOCOL,VERIFICATIONIP,BUSUTILIZATION,ANDCOVERAGEMODEANALYSIS.

INTRODUCTION

The rapid growth in CMOS technology andComputer Aided Design leads to usage oflargenumberofIP(IntellectualPropertyCores) inthe complexdigitaldesigns[1].With the help of these IP cores integration,NowadaystheSOC(SystemonChip) designbecomes more popular and intensively usedfor many applications [2]. Also all the SOCdesignusesbusprotocolsformakingthedata communicationandsynchronization[4-6].Hence the reusability of large number of IPcoresinthecomplexdesignmakesthefunctionalverificationprocesssocrucial(i.e.asitinvolves70%percentofthetimespanascompared to the 30% of the time span fordesign process). In order to overcome thisdifficultyandlargetimespantheverificationengineersproposedamethodologyforverifying the functionality of the chip usingan inbuilt verification environment called asVerificationIP(VIP)[7-10].Normallythebusprotocolsusedinthemodern SOCsare APB(AdvancedPeripheralBus),AHB(Advanced high performance Bus) and AXI(AdvancedExtensibleInterface).Oncomparingthesethreebusprotocols,theAXIbus protocols gives better performance andconsumesmoderatepower.HencealltheSOC design involves the usage of AMBAAXIbusintheinternalarchitecture.Normally in the functional verification, thefailure mode analysis and fault robustness isperformedforthedesign.Forovercomingthesl ag in the functional verification process, averification environment based methodologyisproposedusingSystemVerilogin coverage enabled mode. In this verificationmodeenvironment,thetwooperationarecarried out as i) Proper test-cases are definedfortheDUV(DeviceunderVerification)&ii)Determinethenumberoftest-casestoanalyze and cover all the functionalities ofthe design. During the verification process,the coverage enabled mode easily

identifiesthebugsinthedesignbyidentifyingthecoverageofthecodeandvalidatingthefunctionalbehavior of the design for all testscenarios.

EXISTINGMETHOD

AMBA-AXIBUSARCHITECTURE

AMBA(AdvancedMicrocontrollerbusarchitecture)isanonchipbusprotocolfrom

ARM. It tells about the on chip interconnectspecificationsfortheestablishingtheconnectionbetweentheprocessor,functionalblocksandperipherals.TheAXIbusprotocolarchitectureisthemostsuitableandusableinmodern SOCs and FPGA. This is due to thecharacteristics of large bandwidth capability,interfacingwithcomplexbridges,largememoryaccessandhighbackwardcompatibility with peripherals. Also the AXIbus architecture is having separate read andwritedataphaseswithindividualdatachannels,unaligneddatatransactionsandburst mode access. This section explains thebusarchitectureofAXIprotocolusedfortheddatacommunicationandsynchronizationoperations. In this bus architecture the datatransactionsareestablishedintwophasesastransactionispictorially representedin thefig.1.

i)ReadTransactionphaseandii)WriteTransactionphaseinthebus.Thecorrespondingphasesofoperationareexplainedinthesubsectionswiththe master
–slaveconfigurations.

READTRANSACTIONPHASE

Inthereadtransactionphase,thereadaddress(AR) and read data response(R) signals areinvolvedinthedatacommunicationandsynchronizationprocess.Inthereadtransactionthefirstthevalidaddress(AR)andReadchannelaccessis

communicatedbymastertoinitializethetransactionsandthentheslaverespondswithasignalARready(i.emakingtheaddressreadyforthecommunication).Afterthereception of AR ready the master checks theaddress and then receives the RVALID andread channel data signals. Following to thatthemasterestablishesthechannelcommunicationwithcontrolsignalwithavalidRRreadyandestablishesthereadtransactions. The entirearchitecture/operation of the read

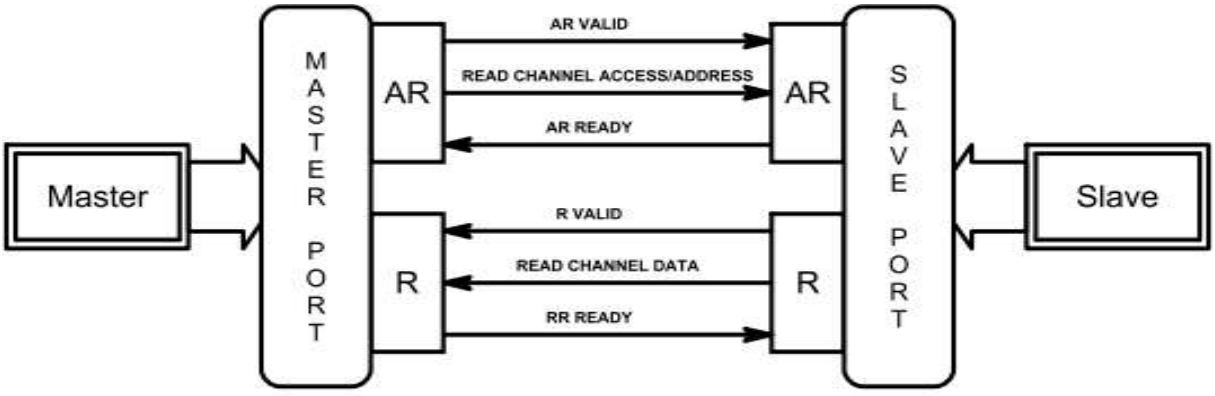


Figure 1: AXI Read Transactions

WriteTransactionPhase

The write transactions are happening in thefollowingthreemodesasi)Writeaddresschannel, ii)Write data channel and iii)Writeresponsechannel.Inthewriteaddresschannelmode,themasterstartsthecommunicationwiththecontrolsignalsAW

VALID and Write channel access/address tothe slave (i.e it sends the valid address andchannelcontroland address).ImmediatelytheslaverespondswithavalidAWready.InthesamemannerduringtheWritedatachannelmode,themasterinitializesthetransactionswithaWVLAIDandWritechanneldata,followingtothattheslaveacknowledges by a valid WREADY signal.Similar to the data and address mode, theWrite response channel mode involves

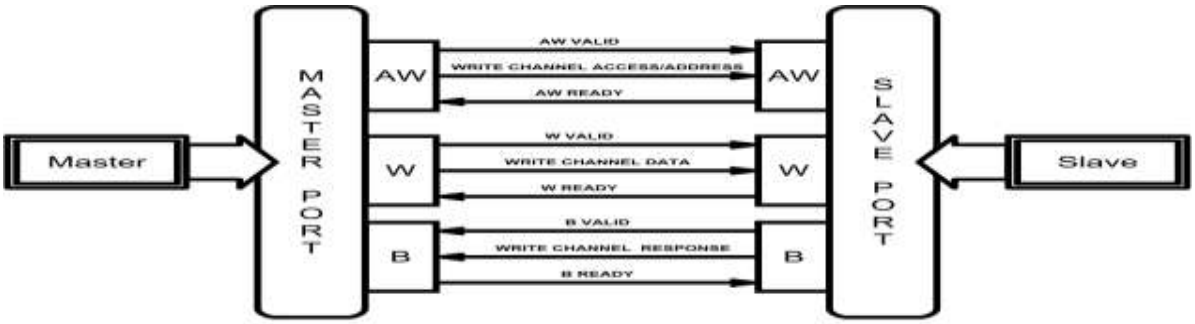


Figure 2: AXI Write transactions

thetransactionstartedbymasterwiththecontrolsignalsBVALIDandwriteresponsechannel.Upon receiving the control signal, the slaveestablishesthecommunicationbyavalidBREADY signal. The operation of the writetransactionsareshown inthefig.2.

PROPOSED VERIFICATIONENVIRONMENT

The verification environment is a standardmethodofverifyingtheDUVincodecoveragemode.Thefollowingcomponents

arepresentintheproposedverificationenvironmenti)Test-suite,ii)Virtualsequencer,iii)Sequencer,iv)Driver,v)AXI-Monitor,vi)Protocolchecker,vii)BusMonitor,viii)CoverageCollectorandxi)Scoreboard.

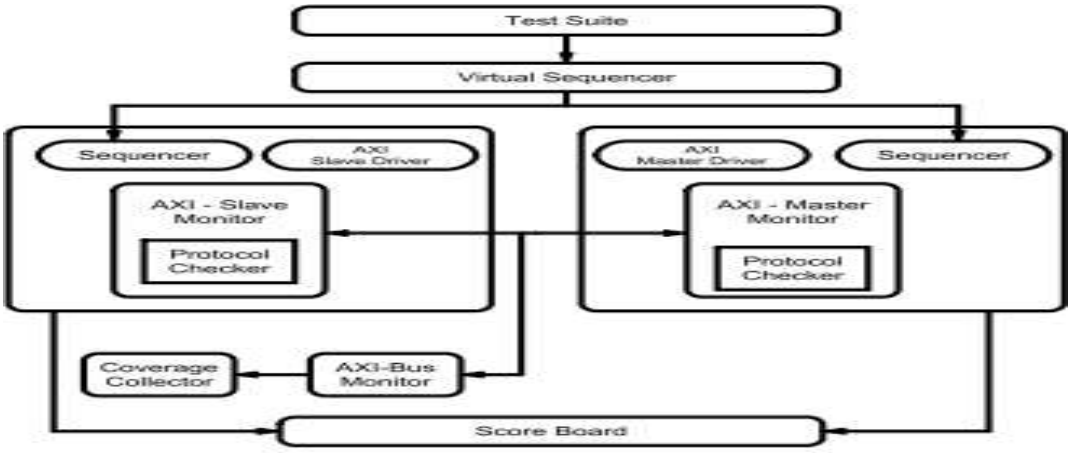


Figure - 3 Verification Environment

Test-Suite: Test-suite consists of all the test-cases for checking the specific key featuresoftheDUVandthefunctionalityinaconstrainedrandommode.Thetest-caseisofthe form constrained random mode or directrandomtest-case.Thetestisregressivelyperformedonthedesignandanalyzed.Itnormallycontainssetofstimulusforrunningthedesign.

Virtual Sequencer: Generallythesequencer generates random sequences forverifying the key properties of the design.Thegeneratedsequenceiscalled astoplevel

sequenceandsplittedintocorrespondinglevel thevirtualsequencerverifiesthefunctionalityof each subcomponent by driving/forcing themwiththeset of sequences.

Sequencer:Sequencerisacomponent,whichgen eratessetofsequences.Thegenerated sequences are of two types activeand passive. The active sequence drives thesignal whereas the passive does not drive thesignal. The sequencer aligns and generatesthe sequence accordingly to the criteria offunctionalitychecks.

Driver:Driveristhecomponentwhichinterfaces or forces all other components torespond accordingly to the feeded stimulus(i.esimplyitdrivestheinputtothecorres pondingblocks).

Monitor: The monitor watches all the datatransactions of the all the components andreports the result to the coverage collector.

IthasaTLMportforanalysisandvirtualinterface to handle the points of the DUVsignals.

Protocol checker: In this module, the DUVfunctionalityisverified,theinterfacecompli anceisalsocheckedwiththetemporalbehaviorof theinputs.Alsotheresponsesaremonitoredforal lthecombinationsoftheinputsequences.

Busmonitor:Busmonitorscreensthefunctionalo perationofindividualcomponentsand connectsthe master/slavemonitor.Finallythetransactionsar ecollectedinthecoveragecollectorasdatabase.

CoverageCollector:Coveragecollectorcollectsal lthecodecoverageinformationlike branch, statement and FSM in the DUVis covered by the specified test-case or not.Normally the verification engineers aim for100%ofcoverageduringthefunctionalverific ation.

VERIFICATIONPLAN

Theverificationplantellsthepropertyhastobeve rifiedanddrivesthecoveragecriteriatobesatisfie d.Agoodplancontainsmeasurablemetrics and successful test-case to achievethe coverage and functionalitycheck. Theplan of verification tells what to be verified,howtoverifyit.InthisAMBAAXIverificati on the properties to be verified arei)System connectivity during read and writecycle, base and primitive sequences. Thus ii)Transaction routing and iii)finallytheDataintegrity.Inthesystemconnecti vitycheckingtest,thesystemintegrationismonit oredbythecorrespondingacknowledgement signals. Then during theroutingstagethebusdataoccupancystructur eisverifiedbythebusutilizationand efficiency. Finally the data integrity is notedfor every transactions and the functionalitycheckpassiscarriedoutforeachofth estage.

In this AXI protocol, the verifications planfocusesthecoverageofthefollowingscenari osas

- **Readphase**
- **WritePhase**
- **Write&ReadPhasefromsameaddress**
- **Write&ReadPhasefromdifferentaddr ess**
- **Overlappedtransactions**

Forthecorrespondingscenariosthetest-casesaregeneratedandthesimulationiscarried out for the functionality verification.Usingthefollowingbusperformanc emetricsValidCount,BusyCountandBusUtilizati onfactor,theperformanceofthebusisassessed.I f the bus is not verified accurately in thecorresponding test-cases, then the test-casesaremodifiedaccordinglytoreachthespecifi cproperty checks. Also in the verification, thecodecoveragebasedverificationmodeanaly sis is carried out for the DUV; if the100% coverage is not achieved during theanalysisthetest-caseisalteredtocoverallthecodeparts ofthedesign.

RESULTS&DISCUSSIONS

Performance evaluations employing quality metrics for data metrics are presented in this part based on AMBA AXI simulation results in five separate test cases. The individual AXI Master/Slave modules are modeled using System Verilog and integrated into the modeled test environment for verification before the simulation analysis can begin. The DUV is integrated with the sequencer, interface, driver, and monitor to evaluate performance in a limited mode in the verification environment. Simulation is

conducted out with the Xilinx ise after the top module integration with DUV. In this example, the

test-case is created to cover five various scenarios, including: I reading, (ii) writing, (iii) reading and writing from the same address, (iv) reading and writing from a different address, and (v) overlapping transactions.

VERIFICATIONOFREADPHASE

In this phase the read data transactions of theAMBAAXIprotocolisverifiedwiththeMaster/ Slaveconfigurationmode.Duringthereadycycle transactionsthesignalsARVALID,ARREADY,RVALID,RREADY,RLAST,RDATAandARSIZE aremonitoredandverified.Herethefunctionality checkprimarilyinvolvestwo modes of operation namely i) Read Addressandii)ReadResponsechannel.Fortheevery positiveedgeofclock,thereadaddresschannelwillfetchtheaddressatthehighstatevaluesofARVALIDandARREADY.Similarlyafteratimedelay, theresponsewillbe instantiated to high mode with the highvaluesofthesignalonRVALIDandRREADY. The last transaction of the readoperation is indicated by the high values ofRLAST.ThevaluesofARSIZEandARLENaremeasuredandindicatethenumberoftransactionsoccurredinreadmode.Forverifyingthereadphaseatest-caseisgeneratedandsimulatedtotestthefunctionalityofthereadoperation.Theworkingoftheread modeincludestwochannelsasexplainedabove withthemeasure of the quality metrics for the readaddress,readchanneldatawithchannelresponse. The entire operation of the readphaseispictoriallyrepresentedasawaveformin thefig.4.

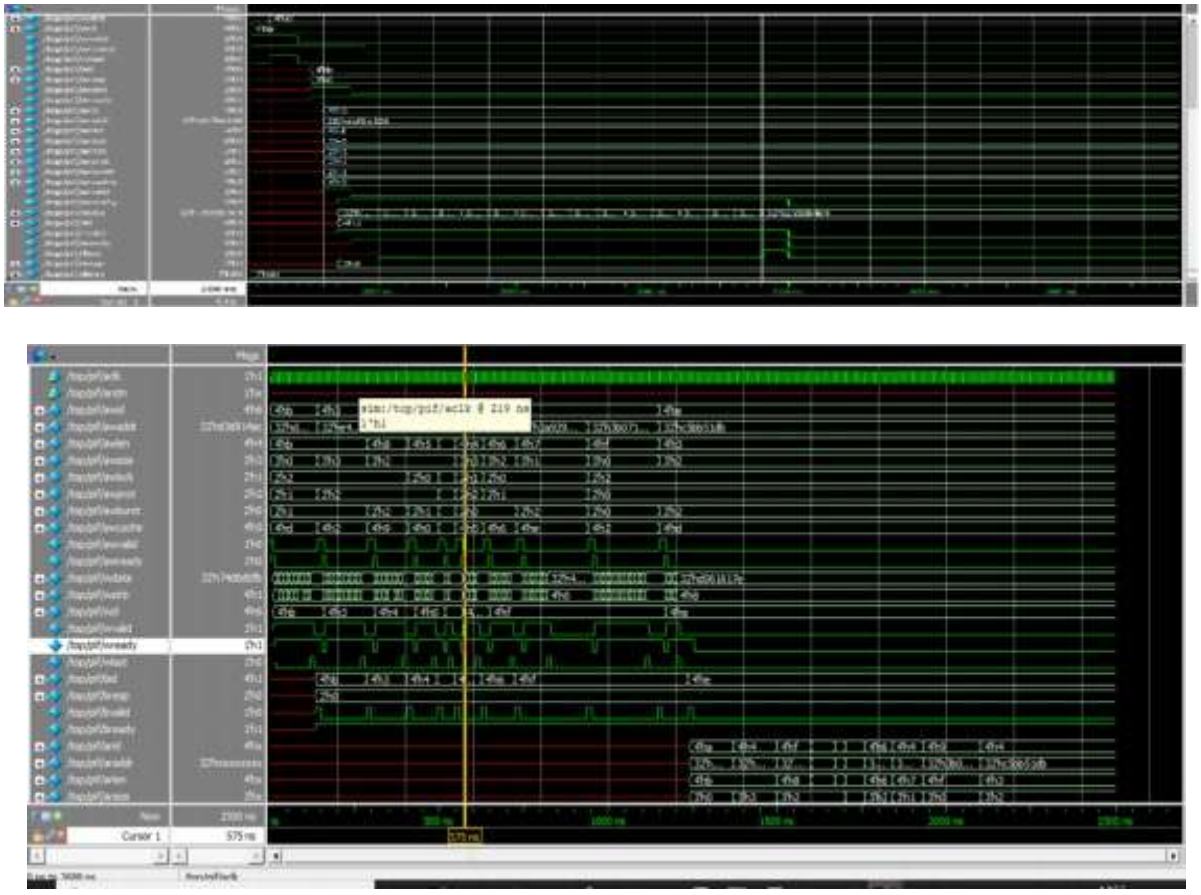
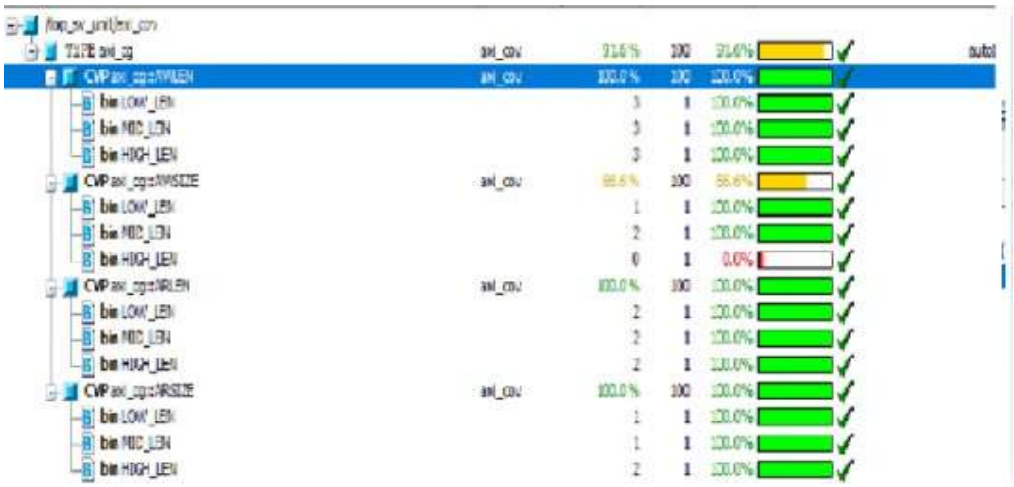


Figure4:ReadPhaseSimulationResponse

VERIFICATIONOFWRITEPHASE



It's just like the Read Phase of the AMBA AXI protocol in that Master/Slave configurations must be verified for AWIDs, AWADDRS, AWLENs, and AWSIZEs. Write Address Channel, Write Channel Data, and Write Response Channel are three of the core operations of the Write Phase. In order to get a valid write address and an acknowledgement AWID on each positive clock cycle, the signals WVALID and WREADY go into high logic state. In the same way, when the BVALID and BREADY transitions are high, the write response operation will occur. Control signals AWLEN and AWSIZE track the size of each transactions, with AWLEN starting at 0000 and incrementing with each new transaction. An illustration of Write Transactions is depicted in the figure 5.

Figure5:WritePhaseSimulationResponse

Thecoveragereportis10writeandreadcompare transaction compare to previous wearemoresignalsarecoveringandalso83.3%wi llbecover thetransactions.

Fig 6:coverage report of 10 write readtransation

Thecoveragereportis16writeandreadtransacti on compare to previous we are moresignals are covering and also 91.3% will becoverthetransactions

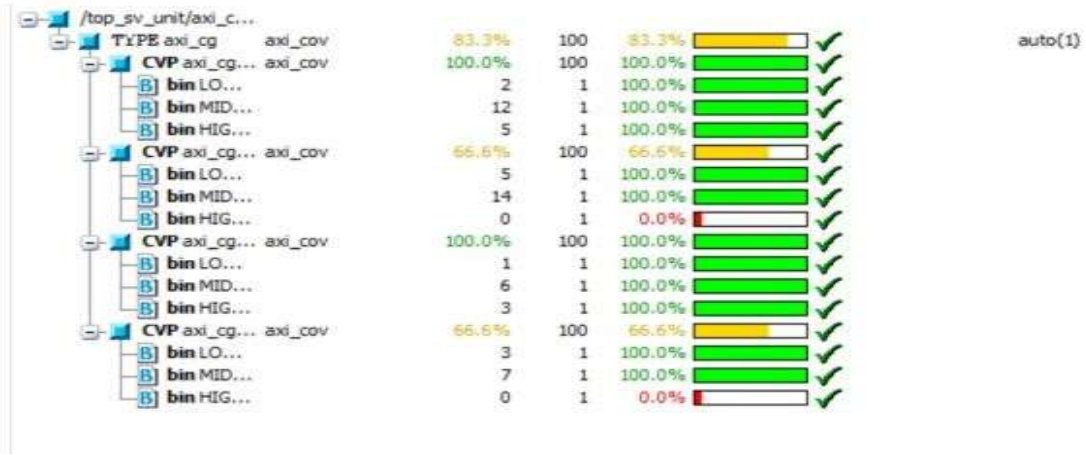


Fig7:coveragereportof16transaction

More signals are being covered, and 75.0 percent of the transactions will be covered according to the coverage report, which compares transactions written and read.

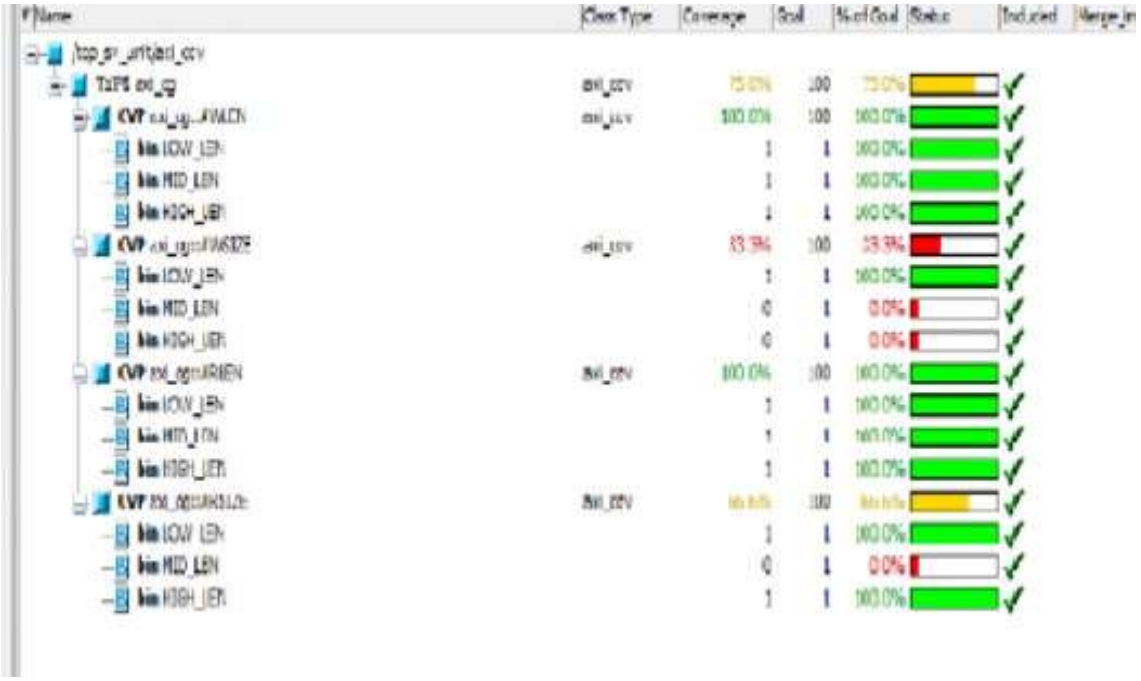


Fig 8: coverage report of 16 transaction repeat2time

CONCLUSION

We introduced a resource allocation algorithm deadlock avoidance condition and an AXI protocol architecture allowing tagged transactions. The proposed RAG simulation results using the AXI protocol can show the extensions for out-of-order transactions (Resource Allocation Graph). The efficiency of the system is increased by utilizing the orbiter techniques and multicasting components.

FUTURESCOPE

Master-slave communication can be improved with the addition of the suggested system's modular componentry. Reduces the complexity of the hardware, making it more useful for system verification.

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